Amendments to the Claims

Please cancel claims 1-13 and 32-46 prior to examination.

Claims 1-13 (Cancelled)

14. (Original) A method of fabricating an array substrate for use in an IPS-LCD device, comprising:

depositing a first metallic material on a substrate;

patterning the first metallic material to form a first gate electrode, a first gate line, a first common line, and a plurality of protrusions, wherein each protrusion has a hole in a central portion thereof and extends from the first common line, and wherein the first gate electrode extends from the first gate line;

depositing a second metallic material on the substrate and on the patterned first metallic material;

patterning the second metallic material to form a second gate electrode, second gate line, second common line, a common-connecting line, and a plurality of common electrodes, wherein the first and second gate electrodes overlap each other to form a double-layered gate electrode, wherein the first and second common lines overlap each other to form a double-layered common line, and wherein the first and second gate lines overlap each other to form a double-layered gate line;

forming a gate insulation layer on the substrate and on the patterned second metallic material;

forming an active layer and an ohmic contact layer sequentially on the gate insulation layer and over the double-layered gate electrodes;

depositing a third metallic material on the ohmic contact layer and on the gate insulation layer;

forming a data line, a source electrode, and a drain electrode by patterning the third metallic material, wherein the source and drain electrodes are over the double-layered gate electrodes, and wherein the data line is perpendicular to both the double-layered gate lines and double-layered common lines;

forming a passivation layer on the patterned third metallic layer and on the gate insulation layer, wherein the passivation layer has a drain contact hole to the drain electrode, and an etching hole over each protrusion;

depositing a transparent conductive material on the passivation layer having the drain contact hole and the etching hole; and

forming a plurality of pixel electrodes and first and second connecting lines.

15. (Currently Amended) A method of fabricating an array substrate according to ~~calim~~claim 14, further comprising: forming a channel region by patterning a portion of the ohmic contact layer between the source and drain electrodes.

16. (Original) A method of fabricating an array substrate according to claim 14, wherein each pair of double-layered gate lines and data lines defines a pixel area.

17. (Original) A method of fabricating an array substrate according to claim 14, wherein the double-layered common line is parallel with and spaced apart from the double-layered gate line.

18. (Original) A method of fabricating an array substrate according to claim 14, wherein a plurality of the common electrodes are parallel with the data line.

19. (Original) A method of fabricating an array substrate according to claim 14, wherein the common-connecting line is perpendicular to and connects the plural common electrodes with each other.

20. (Original) A method of fabricating an array substrate according to claim 14, wherein a plurality of the pixel electrodes are spaced apart from and parallel with the said common electrodes.

21. (Original) A method of fabricating an array substrate according to claim 14, wherein each pixel electrode is located between the pair of common electrodes and corresponds to each common electrode.

22. (Original) A method of fabricating an array substrate according to claim 14, wherein the first and second pixel-connecting lines are parallel with the double-layered common line and respectively connect the pixel electrodes to each other at respective first and second ends of the pixel electrodes.

23. (Original) A method of fabricating an array substrate according to claim 14, wherein the second pixel-connecting line overlaps a portion of the double-layered common line to form a storage capacitor.

24. (Original) The array substrate according to claim 23, wherein the protrusions extended from the first common line are located on both sides of the storage capacitor.

25. (Original) A method of fabricating an array substrate according to claim 14, wherein the double-layered gate electrode, the active layer, the ohmic contact layer, the source electrode and the drain electrode comprise a thin film transistor that is located near the crossing of a double-layer gate line and data line.

26. (Original) A method of fabricating an array substrate according to claim 14, wherein the third metallic material is selected from a group consisting of chromium (Cr), aluminum (Al), aluminum alloy (Al alloy), molybdenum (Mo), tantalum (Ta), tungsten (W), and antimony (Sb).

27. (Original) A method of fabricating an array substrate according to claim 14, wherein the double-layered common line is made of the same material as the double-layered gate lines and formed in the same layer as the double-layered gate lines.

28. (Original) A method of fabricating an array substrate according to claim 14, wherein each protrusion has a quadrilateral shape.

29. (Original) A method of fabricating an array substrate according to claim 14, wherein each protrusion has a quadrilateral-shaped hole in a central portion thereof.

30. (Original) A method of fabricating an array substrate according to claim 14, wherein the first metallic material includes aluminium (Al).

31. (Original) A method of fabricating an array substrate according to claim 14, wherein the second metallic material is selected from a group consisting of molybdenum (Mo), chrome (Cr) and tungsten (W).

Claims 32-46 (Cancelled)